CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1-15. (Canceled)

16.   (Currently Amended) A method of realigning data, said method comprising the steps of:

determining a data alignment of input data comprising a plurality of input bytes <u>coupled to a predetermined number of byte lanes</u>;

generating an input alignment signal indicating a shift required to realign said plurality of input bytes;

<u>coupling input bytes of said plurality of input bytes to a delay multiplexer and a pass multiplexer</u>;

configuring ~~hardware~~ <u>said delay multiplexer and said pass multiplexer</u> according to a shifting configuration based upon said input alignment signal to selectively transfer input data;

realigning said input ~~data in the hardware~~ <u>bytes of said plurality of input bytes using said delay multiplexer and said pass multiplexer</u> based upon said shifting configuration; and

outputting said realigned data <u>comprising a predetermined number of bytes corresponding to said predetermined number of byte lanes</u>.

17.   (Original) The method of claim 16 wherein said step of determining a data alignment of input data comprises a step of determining misaligned data.

18.   (Currently Amended) The method of claim 16 wherein said step of configuring ~~hardware~~ <u>said delay multiplexer and said pass multiplexer</u> to selectively transfer input data comprises a step of configuring programmable hardware to generate an arbitrary byte alignment of said output.

19.   (Currently Amended) The method of claim 16 wherein said step of configuring ~~hardware~~ said delay multiplexer and said pass multiplexer to selectively transfer input data comprises a step of configuring programmable hardware to generate a fixed byte alignment of said output.

20.   (Original) The method of claim 16 further comprising a step of concatenating a second plurality of input bytes with said plurality of input bytes.

21-30. (Canceled)

31.   (Withdrawn) A method of realigning data, said method comprising the steps of:

determining a data alignment of input data comprising a plurality of input bytes;

configuring a delay multiplexer to transfer predetermined bytes of said input data to an output multiplexer;

configuring a pass multiplexer to transfer other predetermined bytes of said input data to said output multiplexer;

realigning said input data using said delay multiplexer; and

outputting said realigned data.

32.   (Withdrawn) The method of claim 31 wherein configuring a delay multiplexer to transfer predetermined bytes of said input data to an output multiplexer comprises configuring said delay multiplexer with X-1 multiplexers, where X equals the number of data bytes transferred by said programmable logic device.

33.   (Withdrawn) The method of claim 31 wherein configuring a pass multiplexer to transfer other predetermined bytes of said input data to the output multiplexer comprises configuring said pass multiplexer with X-1 multiplexers, where X equals the number of data bytes transferred by said programmable logic device.

34.   (Withdrawn) The method of claim 31 further comprising coupling said output multiplexer to said delay register and said pass register.

35.   (Withdrawn) The method of claim 34 wherein coupling said output multiplexer comprises implementing X-1 multiplexers, where X equals the number of data bytes transferred by said programmable logic device.

36.   (Withdrawn) The method of claim 31 further comprising coupling an valid input data signal for each byte lane of a plurality of byte lanes receiving said input data.

37.   (Withdrawn) The method of claim 31 further comprising generating a valid output data signal.

38.   (Withdrawn) The method of claim 31 further comprising generating an input alignment signal indicating a shift required to realign said plurality of input bytes.

39.   (Currently Amended) A method of realigning data, said method comprising the steps of:
        determining a data alignment of input data comprising a plurality of input bytes coupled to a predetermined number of byte lanes;
        coupling input bytes of a plurality of input bytes to a delay multiplexer and a pass multiplexer;
        configuring hardware said delay multiplexer and said pass multiplexer according to a shifting configuration to selectively transfer said input data to align said input data;
        realigning said input data in said hardware bytes of said plurality of input bytes using said delay multiplexer and said pass multiplexer based upon said shifting configuration;
        generating an output word comprising a predetermined number of bytes

corresponding to the predetermined number of byte lanes;

concatenating a plurality of output words having [[a]] said predetermined number of bytes; and

outputting said realigned data.

40.	(Previously Presented) The method of claim 39 further comprising storing a last valid data state to a register.

41.	(Previously Presented) The method of claim 40 further comprising coupling a valid output data byte to said register.

42.	(Previously Presented) The method of claim 39 further comprising receiving a valid input data bit for each byte of input data.

43.	(Previously Presented) The method of claim 39 further comprising coupling a destination alignment signal to a multiplexer control circuit.

44.	(Previously Presented) The method of claim 43 further comprising coupling a data alignment initialization signal to said multiplexer control circuit.

45.	(Previously Presented) The method of claim 44 further comprising generating multiplexer control signals based upon said destination alignment signal and said data alignment initialization signal.